



Inside the AMD Microcode ROM -

(Ab)Using AMD Microcode for fun and security

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> Benjamin Kollenda, Philipp Koppe, Marc Fyrbiak, Christian Kison, Christof Paar, Thorsten Holz

Horst Görtz Institute for IT-Security Ruhr-Universität Bochum <firstname.lastname>@rub.de

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- Crash course: Micro-architecture basics and Microcode
- Reconstructing the Microcode ROM
- Application examples
- Framework overview



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• Firmware for the processor

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 - Fix CPU bugs



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 - Instruction decoding



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 - Complex features (Intel SGX)

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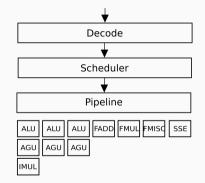
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 - Fix CPU bugs
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 - Complex features (Intel SGX)
- Update capabilities



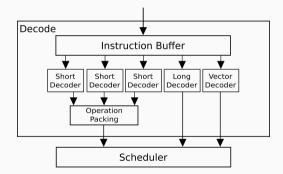
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x86 Instruction Decoding



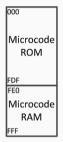






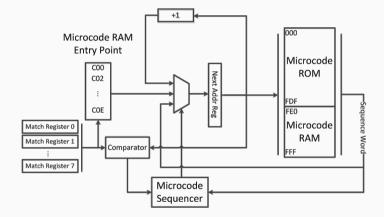




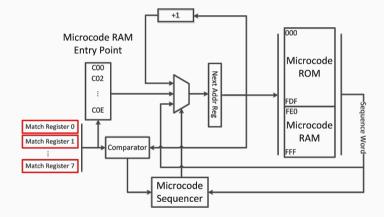


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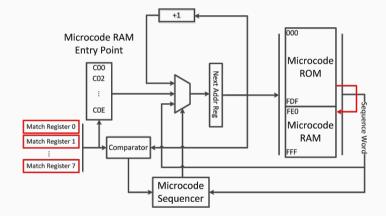












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- Triad structure:

0	6	4 1	28	192 224
	Operation 1	Operation 2	Operation 3	Sequence Word

- Updates protected by weak authentication
- Only one update may be loaded at a time



```
sub eax, edx
sub.C t56q, rcx, 0x100
jcc ECF, 1
.sw_next // implied sequence word if omitted
```

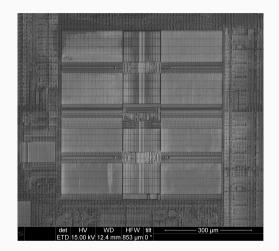
ld t1d, [eax]
st [edx], t1d
mov eax, eax
.sw_complete

mov eax, 1
sub.Q rax, rcx
add.EP t56d, eax, ecx
.sw_branch 0xF01

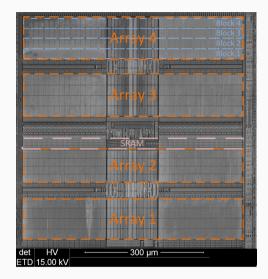


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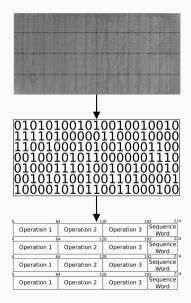






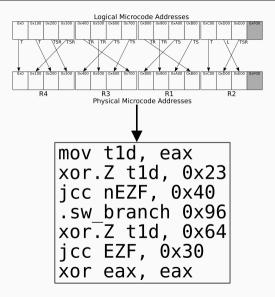
ROM - Recovery Process Overview





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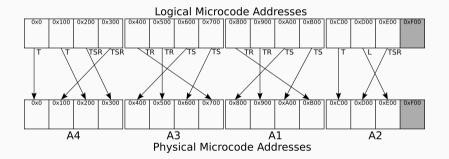
ROM - Mapping Recovery Details

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 - Supports known arithmetic operations
 - Whitelist of no-op operations
- Emulation yielded 54 additional address pairs

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- SHRD 0×ACA
- RDTSC 0x318
- WRMSR 0×6A9



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- Enclave-like execution environment



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```
CheckAddressAndCrashIfBad(Addr, kSize) {
 ShadowAddr = (Addr >> 3) + kOffset;
 if (kSize < 8) {
    Shadow = LoadByte(ShadowAddr);
    if (Shadow && Shadow <= (Addr & 7) + kSize - 1)
     ReportBug(Addr);
 } else {
    Shadow = LoadNBytes(ShadowAddr, kSize / 8);
   if (Shadow) ReportBug(Addr);
 }
}
```

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 - Better performance
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 - Runtime configuration

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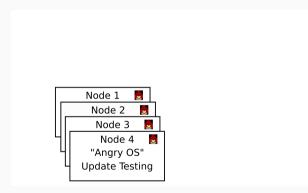
- Implement HWASAN by replacing bound
 - New interface: bound reg, [size]
 - No-op for successful check
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- Single Instruction error check
- No x86 registers needed
- Micro benchmark shows performance advantage (106 vs. 129 cycles)



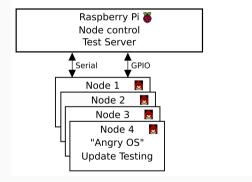


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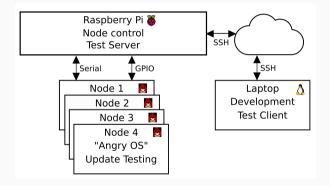








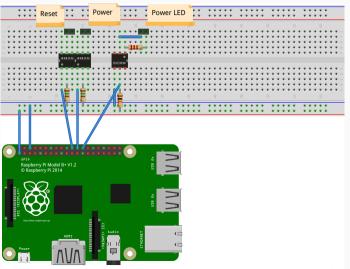














Minimal custom operating system



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- Control 100% of executed instructions



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- Listens for commands on the serial port



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- Control 100% of executed instructions
- Listens for commands on the serial port
- Apply updates, run streamed test code, error reporting



• Microcode assembler and verbose disassembler



- Microcode assembler and verbose disassembler
- x86 assembler to write test code



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- x86 assembler to write test code
- Disassemble existing updates and ROM contents after extraction



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- x86 assembler to write test code
- Disassemble existing updates and ROM contents after extraction
- Create new updates, loadable by Linux update driver
- Control Angry OS node via serial and GPIO
- Remote execution wrapper



- Reversing of the ROM opens up many more possibilities
- Lots left to do, if you want to help, contact us!
- Framework, Angry OS, example programs and more available on Github

https://github.com/RUB-SysSec/Microcode

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